CLAIMS

I claim:

1. A current sense amplifier circuit coupled to detect a first current flowing in a first node, comprising:

an input gain stage incorporating a feedback loop, the first current being coupled to an input node of the input gain stage, wherein the input gain stage operates to maintain the voltage at the input node at a substantially constant level;

a current mirror coupled to an output node of the input gain stage to mirror the first current into a second current;

a charge integration stage coupled to integrate charge associated with the second current to develop a first voltage; and

a comparator coupled to compare the first voltage to a reference level and providing an output signal at an output terminal,

wherein the comparator generates an output signal having a first value when the first current exceeds a predetermined threshold level and a second value when the first current is less than the predetermined threshold level.

2. The current sense amplifier circuit of claim 1, wherein the input gain stage comprises:

a first transistor having a control terminal being the input node, a first current handling terminal coupled to receive a first bias current, and a second current handling terminal coupled to a first power supply voltage; and

a second transistor having a control terminal coupled to the first current handling terminal of the first transistor, a first current handling terminal coupled to the current mirror

and being the output node of the input gain stage, and a second current handling terminal coupled to the input node,

wherein the first transistor is biased to conduct a current substantially equal to the first bias current, and the second transistor forms the feedback loop to maintain the voltage at the input node at a substantially constant level.

3. The current sense amplifier circuit of claim 2, wherein the input gain stage comprises a unity gain input gain stage.

4. The current sense amplifier circuit of claim 2, wherein the input gain stage further comprises:

a third transistor having a control terminal and a first current handling terminal both coupled to the input node, and a second current handling terminal coupled to the first power supply voltage; and

a current source coupled to provide a second bias current to the first current handling terminal of the second transistor,

wherein the third transistor conducts a current substantially equal to the current being conducted by the first transistor and the second bias current is at least as large as the current being conducted in the third transistor.

5. The current sense amplifier circuit of claim 1, wherein the current mirror comprises:

a fourth transistor having a control terminal and a first current handling terminal coupled to the output node of the input gain stage and receiving the input current, and a second current handling terminal coupled to a second power supply voltage; and

a fifth transistor having a control terminal coupled to the control terminal of the fourth transistor, a first current handling terminal coupled to a second node and providing the second current, and a second current handling terminal coupled to the second power supply voltage.

6. The current sense amplifier circuit of claim 1, wherein the charge integration stage comprises:

a first capacitor having a first plate coupled to receive the second current and a second plate coupled to the first power supply voltage.

7. The current sense amplifier circuit of claim 6, wherein the charge integration stage further comprises:

a sixth transistor having a control terminal receiving a first pulse, a first current handling terminal coupled to the first plate of the first capacitor and a second current handling terminal coupled to the first power supply voltage,

wherein the first pulse is selectively applied to discharge the first capacitor.

8. The current sense amplifier circuit of claim 7, wherein the charge integration stage further comprises:

a pulse generator generating the first pulse based on a clock signal, the first pulse having a pulse width that is a fraction of the clock period of the clock signal,

wherein the clock signal determines when the current sense amplifier provides a signal indicative of the output signal of the comparator and the first pulse is generated for each clock cycle to discharge the first capacitor.

9. The current sense amplifier circuit of claim 7, wherein the first pulse has a pulse width that is less than 10% of the clock period of the clock signal.

10. The current sense amplifier circuit of claim 1, wherein the comparator comprises: a comparator with hysteresis, the comparator having a first reference level for detecting a low-to-high transition and a second reference level for detecting a high-to-low transition, the first voltage being compared with a selected one of the first or second reference level.

11. The current sense amplifier circuit of claim 1, wherein the comparator comprises:

a Schmitt trigger having a first trigger point defining the reference level, the Schmitt trigger receiving the first voltage as an input voltage and providing the output signal having the first value when the first voltage exceeds the first trigger point of the Schmitt trigger.

12. The current sense amplifier circuit of claim 11, wherein the Schmitt trigger comprises an inverting stage and the comparator further comprises an inverter having an input terminal coupled to receive the output signal of the Schmitt trigger and generating a second output signal having an inverse logical value as the output signal.

13. The current sense amplifier circuit of claim 1, further comprising:

an output stage for receiving a signal corresponding to the output signal of the comparator and providing a second output signal based on a clock signal.

14. The current sense amplifier circuit of claim 13, wherein the output stage comprises a D-flip flop receiving the signal corresponding to the output signal of the comparator and the clock signal as input signals, the D-flip flop providing the second output signal based on the clock signal.

15. The current sense amplifier circuit of claim 4, further comprising:

a variable current source coupled to receive a bias voltage and generate the first and second bias currents based on the bias voltage.

16. The current sense amplifier circuit of claim 4, further comprising:

a seventh transistor having a control terminal coupled to receive a bias voltage, a first current handling terminal coupled to a third node and a second current handling terminal coupled to the first power supply voltage, wherein the bias voltage causing the seventh transistor to conduct a reference current; and

a first circuit coupled to the third node to generate the first and second bias currents based on the reference current.

17. The current sense amplifier circuit of claim 16, wherein the seventh transistor comprises a long channel length transistor.

18. The current sense amplifier circuit of claim 17, wherein the seventh transistor comprises a pair of serially connected transistors.

19. The current sense amplifier circuit of claim 16, wherein the first circuit comprises:

an eighth transistor having a control terminal and a first current handling terminal coupled to the third node, a second current handling terminal coupled to the second power supply voltage;

a ninth transistor having a control terminal coupled to the third node, a first current handling terminal providing the first bias current and a second current handling terminal coupled to the second power supply voltage; and

a tenth transistor having a control terminal coupled to the third node, a first current handling terminal providing the second bias current and a second current handling terminal coupled to the second power supply voltage,

wherein the ninth transistor and the eighth transistor form a second current mirror and the magnitude of the first bias current is a function of the reference current and the size ratio of the ninth transistor and the eighth transistor, and the tenth transistor and the eighth transistor form a third current mirror and the magnitude of the second bias current is a function of the reference current and the size ratio of the tenth transistor and the eighth transistor, the third current mirror being the current source generating the second bias current.

20. The current sense amplifier circuit of claim 16, further comprising:

a resistor coupled between the third node and a fourth node; and

a second capacitor coupled between the fourth node and the first current handling terminal of the first transistor,

wherein the resistor and the second capacitor provide frequency compensation for the input gain stage.

21. The current sense amplifier circuit of claim 5, further comprising:

a pull-up device coupled to the output node of the input gain stage and being controlled by the output signal of the comparator,

wherein in response to the output signal of the comparator having the first value, the pull-up device drives the voltage at the output node of the input gain stage to the second power supply voltage.

22. The current sense amplifier circuit of claim 5, further comprising:

an eleventh transistor having a control terminal coupled to the output terminal of the comparator, a first current handling coupled to the output node of the input gain stage, and a second current handling terminal coupled to the second power supply voltage, wherein the eleventh transistor and the fourth transistor are of the same conductivity type.

23. The current sense amplifier circuit of claim 5, where in the current mirror further comprises:

a first plurality of transistor pairs, each transistor pair including a first transistor and a second transistor being serially connected between the second node and the second power supply voltage, the control terminal of the first transistor of the transistor pair is coupled to the control terminal of the fourth transistor, and the control terminal of the second transistor of the transistor pair is coupled to receive a corresponding one of a plurality of select signals,

wherein the first transistors in the plurality of transistor pairs are selectively turned on based on the

plurality of select signals to provide the second current in conjunction with the fifth transistor.

24. The current sense amplifier circuit of claim 23, wherein the first transistors in the plurality of transistor pairs have different size ratios with respect to the fourth transistor.

25. The current sense amplifier circuit of claim 16, further comprising:

a twelfth transistor having a control terminal coupled to receive the bias voltage, a first current handling terminal coupled to a fifth node and a second current handling terminal coupled to the first power supply voltage; and

a thirteenth transistor having a control terminal coupled to receive a select signal, a first current handling terminal coupled to the third node and a second current handling terminal coupled to the fifth node,

wherein the thirteenth transistor is selectively turned on based on the select signal to multiply the magnitude of the reference current.

26. The current sense amplifier circuit of claim 25, wherein the seventh transistor and the twelfth transistor have a first size ratio and the twelfth transistor conducts a current that is a multiple of the current conducted by the seventh transistor, the sum of the currents conducted by the seventh transistor and the twelfth transistor is the reference current.

27. The current sense amplifier circuit of claim 19, wherein the eighth, ninth and tenth transistors are oversized to increase the matching of the transistors.

28. The current sense amplifier circuit of claim 27, wherein the reference current is increased in accordance with the size of the eighth, ninth and tenth transistors.

29. The current sense amplifier circuit of claim 27, further comprising:

a resistor coupled between the third node and a sixth node;

a first MOS capacitor including a gate terminal coupled to the sixth node and first and second current handling terminals coupled to the first current handling terminal of the first transistor; and

a second MOS capacitor including a gate terminal coupled to the first current handling terminal of the first transistor and first and second current handling terminals coupled to the sixth node,

wherein the resistor and the first and second MOS capacitors provide frequency compensation.

30. The current sense amplifier circuit of claim 1, wherein the current mirror comprises:

a fourth transistor having a control terminal coupled to a seventh node, a first current handling terminal coupled to the output node of the input gain stage and receiving the input current, and a second current handling terminal coupled to a second power supply voltage;

a fifth transistor having a control terminal coupled to the seventh node, a first current handling terminal coupled to a second node and providing the second current, and a second current handling terminal coupled to the second power supply voltage;

a fourteenth transistor having a control terminal coupled to the output node of the input gain stage, a first current handling terminal coupled to a fourth current mirror, and a second current handling terminal coupled to the second power supply voltage; and

a fifteenth transistor having a control terminal and a first current handling terminal coupled to the seventh node and to an output node of the fourth current mirror, and a second current handling terminal coupled to the second power supply voltage.

31. The current sense amplifier circuit of claim 30, wherein the fourteenth transistor is turned on when an input current flows in the input gain stage and conducts a third current into the fourth current mirror, the fourth current mirror provides a fourth current at the output node driving the fifteenth transistor, the fourth transistor mirrors the fourth current flowing in the fifteenth transistor into the output node of the input gain stage, and the fifth transistor mirrors the current flowing in the fourth transistor into the second node.

32. The current sense amplifier circuit of claim 30, wherein the fourth current mirror comprises:

a sixteenth transistor having a control terminal and a first current handling terminal coupled to the first current handling terminal of the fourteenth transistor, and a second current handling terminal coupled to a first power supply voltage; and

a seventeenth transistor having a control terminal coupled to the control terminal of the sixteenth transistor, a first current handling terminal coupled to the seventh node

and a second current handling terminal coupled to a first power supply voltage.

33. The current sense amplifier circuit of claim 30, wherein the current mirror further comprising:

a resistor coupled between the seventh node and an eighth node; and

a third capacitor coupled between the eighth node and the output node of the input gain stage,

wherein the resistor and the third capacitor provide frequency compensation.

34. The current sense amplifier circuit of claim 30, further comprising:

a first pull-up device coupled to the output node of the input gain stage and being controlled by the output signal of the comparator; and

a second pull-up device coupled to the seventh node of the current mirror and being controlled by the output signal of the comparator,

wherein in response to the output signal of the comparator having the first value, the first and second pull-up devices drives the voltage at the output node of the input gain stage and the seventh node, respectively, to the second power supply voltage.

35. The current sense amplifier circuit of claim 30, further comprising:

an eleventh transistor having a control terminal coupled to the output terminal of the comparator, a first current handling coupled to the output node of the input gain stage, and a second current handling terminal coupled to the second

power supply voltage, wherein the eleventh transistor and the fourth transistor are of the same conductivity type; and

an eighteenth transistor having a control terminal coupled to the output terminal of the comparator, a first current handling coupled to the seventh node, and a second current handling terminal coupled to the second power supply voltage, wherein the eighteenth transistor and the fourth transistor are of the same conductivity type.

36. A method for sensing a first current flowing in a first node, comprising:

coupling the first current to an input node of an input gain stage and providing the first current at an output node of the input gain stage;

providing a feedback loop in the input gain stage to maintain a voltage at the input node at a substantially constant level;

mirroring the first current into a second current;

integrating charge associated with the second current at a second node;

developing a first voltage at the second node as a result of integrating the charge associated with the second current;

comparing the first voltage to a reference level;

providing an output signal having a first value when the first voltage exceeds the reference level; and

providing an output signal having a second value when the first voltage is less than the reference level.

37. The method of claim 36, wherein coupling the first current to an input node of an input gain stage comprises coupling

the first current to an input node of a unity gain input gain stage.

38. The method of claim 36, further comprising:

providing the output signal based on a clock signal;

discharging the first voltage at the beginning of each clock cycle of the clock signal.

39. The method of claim 36, further comprising:

in response to the output signal having the first value, driving a voltage at the output node of the input gain stage to a first power supply voltage.

40. The method of claim 36, wherein mirroring the first current into a second current comprises:

in response to the first current being provided at the output node of the input gain stage, conducting a third current in a third node;

mirroring the third current into a fourth current at a fourth node;

providing a negative feedback loop to mirror the fourth current into the output node of the input gain stage; and

mirroring the current flowing at the output node of the input gain stage into the second current.

41. The method of claim 40, further comprising:

in response to the output signal having the first value, driving a voltage at the fourth node to a first power supply voltage.